# A W-BAND MONOLITHIC MEDIUM POWER AMPLIFIER

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*Abstract* — **This paper summarizes the design and measured performance of a MMIC power amplifier for W-Band. The chip was fabricated on a 50 μm GaAs substrate using 0.1 μm AlGaAs/InGaAs/GaAs pseudomorphic-HEMT technology. Measurements show that it has small-signal gain of 19±1 dB from 72 to 95 GHz. During scalar measurements with moderate heat-sinking, the chip delivered more than 100 mW between 75 and 93 GHz, with a corresponding large signal gain of 11 dB. Such an amplifier is widely useful in millimeter-wave applications requiring moderately high power over broad frequency ranges, including emerging wireless communication systems in W-Band.**

## I. INTRODUCTION

Power amplifier device technology and circuit design is now one of the most heavily researched subjects in the fields of microwave and millimeter-wave engineering. Much of a system's architecture and ultimate performance hinges on the available power and efficiency of its signal source. In particular, new applications in W-Band, such as automotive radar, millimeter-wave imaging, and even communications are driving the research forward. Recent developments in MMIC W-Band PA's have shown output powers approaching 0.5 W at 95 GHz [1], and power-added efficiencies of almost 20% [1]-[2].

However, in the race to establish new records for output power, the trend of circuit designers has been toward narrow-band designs, requiring highly-customized chips to be developed for each new application at great cost. The role of a more general purpose, medium power amplifier has been largely neglected. A literature search has only turned up one reference fitting those requirements, wherein two InP MMIC amplifiers are reported, covering 65-145 GHz and 75-110 GHz, with power outputs of 25 mW and 50 mW, respectively [3].

Here, we present design and test results of a 75-95 GHz medium power amplifier with 100 mW power capability, and associated large-signal gain of 11 dB. This amplifier would be useful for millimeter-wave applications requiring moderately high power over a broad frequency range.

## II. CIRCUIT DESIGN

A photograph of the chip appears in Figure 1. The circuit was fabricated at TRW on a 50 μm GaAs substrate using 0.1 μm AlGaAs/InGaAs/GaAs pseudomorphic-HEMT technology. The circuit dimensions are 2600 x 840 μm.

The MMIC amplifier is a 3-stage design with 1, 2, and 4 identical transistor cells in each stage, sequentially. This geometric increase in gate periphery from stage to stage ensures that the output transistors will enter compression

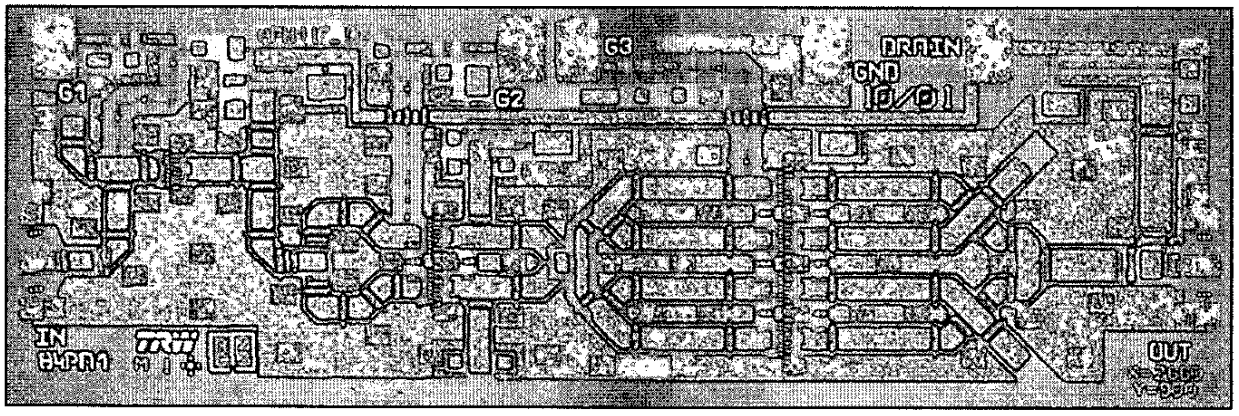


Fig. 1. Photograph of the MMIC PA. Circuit dimensions are 2.6 x 0.84 mm. GaAs substrate is 50 μm thick.



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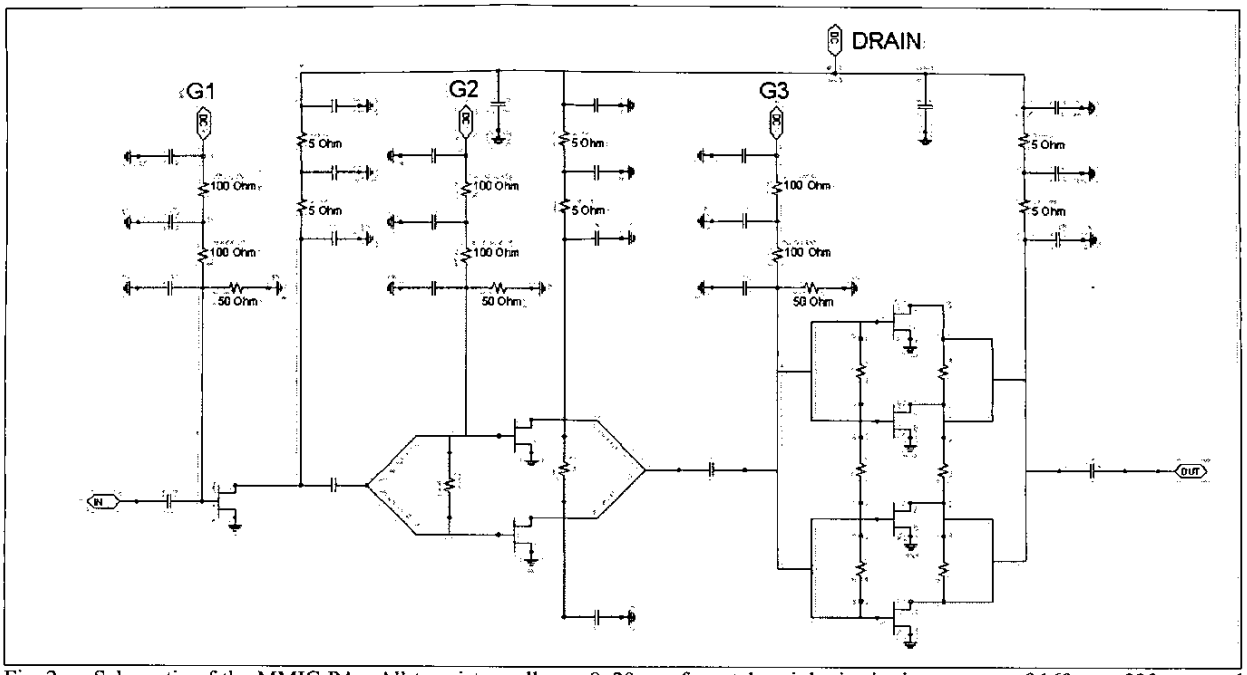


Fig. 2. Schematic of the MMIC PA. All transistor cells are 8x20 μm for total peripheries in three stages of 160 μm, 320 μm, and 640 μm.

first as long as the preceding stages have at least 3 dB gain. All transistor cells are 8-finger devices with 20 μm gate widths, resulting in 640 μm total output periphery for the chip. A small-signal model of this device was extracted from on-wafer measurements of calibrated test-structures below 50 GHz.

The circuit is designed with grounded coplanar-waveguide (GCPW) technology. The advantage of this approach over microstrip layouts is the availability of low-inductance connections to ground. Via holes were placed at less than quarter wavelength spacing to suppress parallel-plate modes in the substrate. Air-bridges were used at all asymmetric discontinuities to prevent the odd-mode from propagating.

A schematic of the circuit is shown in Figure 2. The inter-stage networks consist of coupling capacitors, gate and drain bias lines, stub matching networks, and CPW power combiners and splitters. All transistors are power combined after each stage before re-dividing for the next stage. This facilitates DC bias, since one pair of gate and drain bias supplies can then be shared among all transistors in each stage. The final power combiner consists of low-impedance transmission lines with shunt capacitive stubs connected at the intermediate junctions between transistor pairs. Balancing resistors were incorporated as closely as possible to the transistors in all combiners and splitters to suppress odd-mode oscillations.

Resistors were also placed in the gate and drain bias lines to improve low-frequency stability, which is a frequent problem with W-Band amplifiers. While it degrades the efficiency, this approach was successful in making the chip easier to use, since it has never shown signs of oscillation under any bias condition, drive level, or packaging environment in which it has been tested. The gate bias lines have two 100 Ω resistors in series and one 50 Ω shunt resistor, forming a 5:1 voltage divider. Bypass capacitors short-out these resistors in-band, and isolate the rest of the amplifier from the power supply. The drain lines have much smaller series resistors, 5 Ω, and no shunt element except the bypass capacitors described above.

## III. Measurements

On-wafer, small-signal measurements were performed using an HP 8510C Vector Network Analyzer with WR-10 waveguide extensions from Oleson Microwave Labs. The VNA extenders from Oleson enable 2-port measurements with good dynamic range across the full waveguide bandwidth. Calibration was performed at the probe tips using CPW calibration standards on an Alumina substrate.

The results are plotted in Figure 3. The data shows that the amplifier has small-signal gain of 19±1 dB from 72 to 95 GHz. Output return loss is better than 5 dB

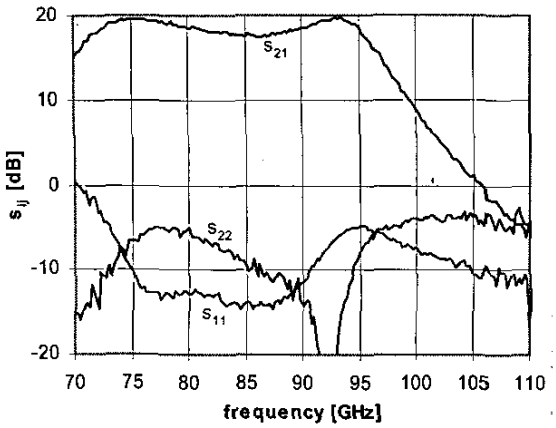


Fig. 3. S-Parameters for the amplifier. $V_G$ = -0.15 V, $V_D$ = 2.5 V, and $I_D$ = 280 mA.

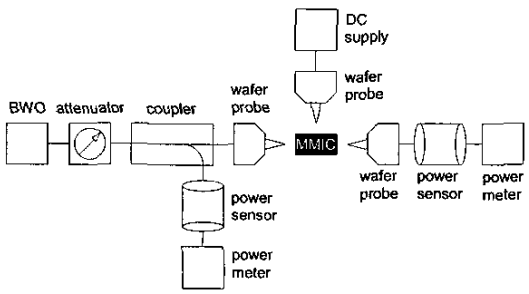


Fig. 4. Diagram of the large-signal measurement setup. The input signal was provided by a Backward-Wave Oscillator. The chip was mounted on a small metal plate for heat-sinking.

across the band, while input return loss exceeds 10 dB from 75 to 90 GHz. The input return loss gets close to 0 dB at 70 GHz, but the measurement could be a few dB off because of calibration errors that occur outside the WR-10 band. In spite of the highly reflective input below band, the amplifier remained stable even when packaged.

Large-signal measurements were also done using a Backward Wave Oscillator as the source. A diagram of this test setup is shown in Figure 4. Immediately following the BWO is a precision attenuator for controlling the power level, which is monitored by a power meter connected through a 10 dB directional coupler. Another power meter on port 2 measures the output power. The signal is coupled into and out of the chip through the same wafer probes that were used during the s-parameter measurements. In this case,

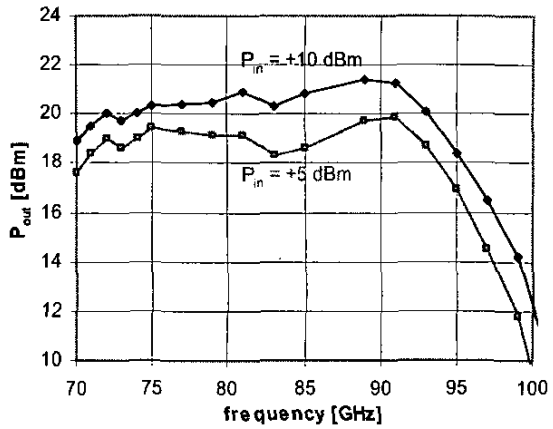


Fig. 5. Output power versus frequency for different input powers. $V_{G1}$ = 0 V, $V_{G2}$ = $V_{G3}$ = -0.3V, $V_D$ = 5 V, $I_D$ = 320-360 mA.

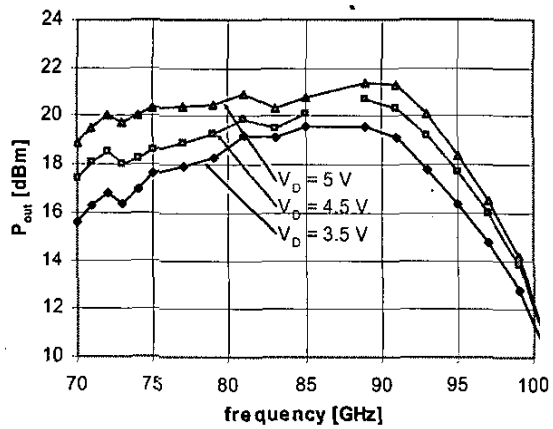


Fig. 6. Output power versus frequency for several bias voltages. Input power was fixed at +10 dBm. $I_D$ = 250-350 mA.

however, the insertion loss of the probes had to be calibrated out manually. This was done using data supplied by the probe manufacturer and verified by landing the probes on a short microstrip through-line. The loss of the interconnecting waveguides were also measured and calibrated out of the measurements so that the data represents the power levels at the ports of the chip. The MMIC was epoxied to a copper plate for heat-sinking during these measurements.

Figures 5 and 6 show the output power versus frequency for various input powers and bias levels. For +10 dBm input power and $V_D$ = 5 V, the chip delivered more than 100 mW from 75 to 93 GHz, with a corresponding large-signal gain of 11 dB. Peak PAE

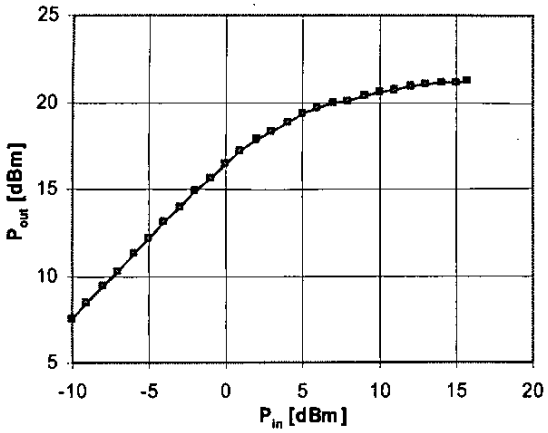


Fig. 7. Output power versus input power at 91 GHz. $V_{G1} = V_{G2} = 0$ V, $V_{G3} = -1.5$ V, $V_D = 4.5$ V, $I_D = 285 - 300$ mA. $P_{1dB} = 16.5$ dBm.

was about 8%.

Output power versus input power at 91 GHz is shown in Figure 7. The power saturated at about 130 mW. This data also shows that the 1 dB compression point is +16.5 dBm.

## IV. Conclusions

Design and test data for a broadband medium power MMIC amplifier in W-Band has been reported. The chip delivers greater than 100 mW of power from 75 to 93 GHz with a large-signal gain of 11 dB and peak PAE of 8%. It is stable under all bias and operating conditions at which it has been tested. The amplifier has potential uses in many applications that require moderate power over relatively wide frequency ranges.

## Acknowledgement

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